



A Novel Multi-Wafer Microfluidic System Architecture for Biomedical Applications (paper)

The process of replicating, or "amplifying" DNA is an integral part of virtually every nucleic acid based test or reaction performed. The polymerase chain reaction, PCR, the most widely practiced amplification technique, is performed more than one billion times every year.

This paper discusses a novel approach proposed by Thermal Gradient and developed collaboratively with Infotonics Technology Center to address several shortcomings of current techniques.

WORLD-CLASS
MEMS INNOVATION

A NOVEL MULTI-WAFER MICROFLUIDIC SYSTEM ARCHITECTURE FOR BIOMEDICAL APPLICATIONS

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INTRODUCTION

The process of replicating, or "amplifying" DNA is an integral part of virtually every nucleic acid based test or reaction performed. The polymerase chain reaction, PCR, the most widely practiced amplification technique, is performed over 1 billion times every year. This process involves repeated thermal cycling of the sample through three temperatures with a resultant doubling of the target DNA with each cycle. Conventional single chamber methods used to perform amplification can be complicated, large, cumbersome, and slow due to the time required to change the temperature of the large thermal mass of the thermocycling tool.

Microfluidic chips have been proposed as a means of decreasing the time for PCR by reducing both the thermal mass of the device and the volume of sample being amplified. The microfluidic devices which have been studied typically have a planar architecture in which the sample fluid travels between three separate temperature zones whose temperatures are maintained by on-chip heaters or block heaters upon which the device sits [1-3]. On-chip heaters introduce additional cost and complication into the fabrication of the PCR chip. Block heaters are inefficient with glass-based PCR devices because of the low thermal conductivity of glass.

These shortcomings have been addressed by a small start-up company, Thermal Gradient, Inc. which proposed a novel externally heated five-layer miniaturized rapid PCR microsystem. The design specifications, operation, and performance of this device are as yet proprietary, and will be presented by Thermal Gradient at a later time. In this paper we describe the microfluidic architecture and process used to microfabricate the five-level microfluidic chip at the heart of the system. This microfluidic architecture has broader application to microfluidic systems for other applications such as miniaturized biological and chemical reactors and sensors.

EXPERIMENTAL APPROACH

The layout of the device is shown in Figure 1. This 4 micro-liter device consists of three high thermal conductance layers containing microfluidic channels separated by low thermal conductance layers containing vias which connect the microchannels on each of the other layers. Fluid is introduced into the top layer where it traverses one of the microchannels, circulates to a channel on the bottom layer, then to a channel on the middle layer, and finally returns to the next channel on the top layer where the cycle is repeated.

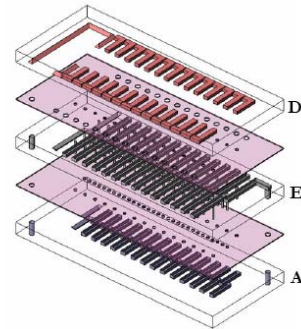


Figure 1. Exploded schematic drawing of the five-layer microfluidic device.

The device was fabricated using silicon wafer processing and wafer-scale bonding at the Infotonics Technology Center's 150 mm wafer fab. Each device was 5 mm x 12 mm, so over 200 chips can be produced with each wafer stack. The multilayer PCR chips were assembled by interleaving microfabricated wafers and patterned polyimide films. Silicon was chosen for the high thermal conductivity

layers because its ease of fabrication permits quick turnaround times for new design prototyping. Double-side-polished silicon wafers 575-um thick were used to enable photolithography and etching on both sides of each wafer. Polyimide was chosen for the low conductivity spacer. Polyimide layers 100 um thick were required to provide the desired thermal conductance.

A schematic of the process flow for one of the three wafers is shown in Figure 2. Similar process flows were applied to each of the three wafers. The wafers were thermally oxidized, photolithographically patterned and dry-etched in a LAM 4250 XLS reactive ion etcher to provide a hard etch mask for channel patterning. An anisotropic KOH wet etch was then used to pattern the the microchannels on each wafer. The resulting channels were triangular in cross-section, approximately 150 um wide and 170 um deep. The patterned wafers are then stripped of oxide in a buffered oxide etch. Handle wafers were coated with photoresist and bonded to the patterned side of the wafers so they could flipped and patterned on the opposite side. This bonded handle wafer protects the microchannels, but also protects the electrode of the etcher during the subsequent through-wafer via etch. The wafers are coated, and the vias are patterned photolithographically. A thick (7 um) photoresist coat is required to ensure its survival during the long through wafer via etch. This etch consists of a 575 um silicon deep reactive ion etch (DRIE) in an STS Advanced Silicon Etcher.

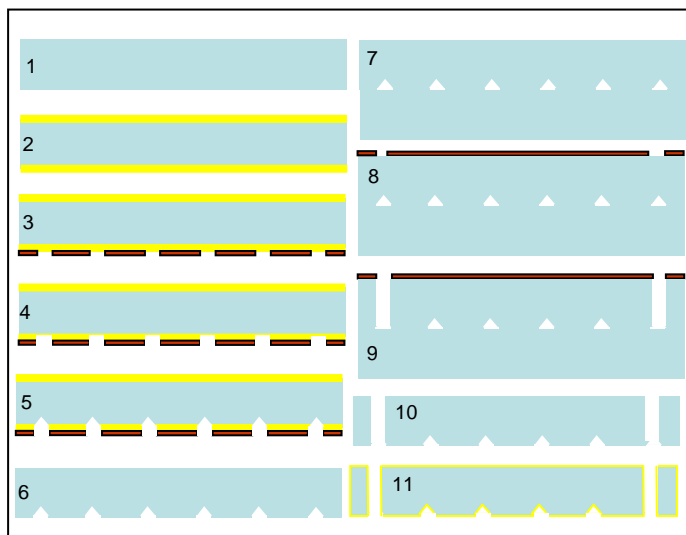


Figure 2. Silicon process steps. 1) Start 575 um Double Side Polish Si Wafers. 2) Thermal oxidation (2 um). 3) Backside photolithography. 4) Backside oxide dry etch (2 um). 5) KOH Etch Channels. 6) Strip photoresist and oxide. 7) Attach handle wafer with photoresist. 8) Frontside photolithography. 9) Through-wafer Si DRIE. 10) Strip resist / remove handle. 11) Thermal oxidation (2500 A).

When wafer patterning is complete, the handle wafers are detached in a solvent or piranha bath that dissolves the photoresist between the wafers. Finally the wafers are re-oxidized with 500-2500 A of oxide to provide a biologically and chemically inert channel surface. The wafers are then ready for assembly.

In parallel vias are patterned in the polyimide films using laser ablation. The wafer surfaces are cleaned and activated using an oxygen plasma. An epoxy adhesive is applied using a mylar transfer process. In this way adhesive is applied only to the flat surfaces of the wafer and no adhesive enters the channels or vias. The wafers and

polyimide films are stacked and aligned on a mechanical fixture designed at Infotonics for this task. Alignment tolerances of 10-12 um are achievable with this mechanical alignment method. The stack is then placed in a vacuum laminator in which pressure and heat are applied to bond the wafers and polyimide films together. Finally the wafer stack is diced into individual PCR chips. Figure 3 is a scanning electron micrograph (SEM) of a cross-section through one of the chips. The vertical vias and intersected anisotropically etched channels can be seen.

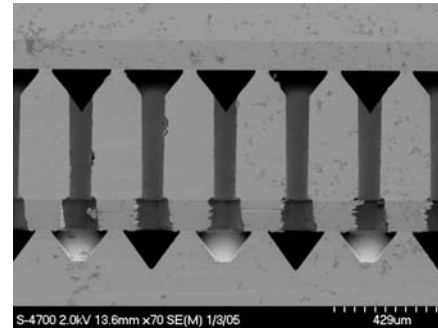


Figure 3. SEM Cross-section of completed device.

RESULTS AND FUTURE WORK

This initial design has been successfully tested by Thermal Gradient. Experiments are underway to develop protocols to further reduce the PCR times. As state earlier, Thermal Gradient will report on these tests at a later date.

Efforts are currently underway to simplify the process flow. The use of the KOH etch required that the channels be patterned before the vias to avoid attack of the vias by the KOH etch. The resulting wafers were fragile, and, as we have seen, require the use of a handle wafer to protect the channels and etcher during the Si DRIE. The new process being developed uses all dry etching, allowing the channels to be fabricated last. This dry etch approach will produce channels with square cross-sections which will provide both better channel uniformity and a larger thermal contact area for the sample.

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